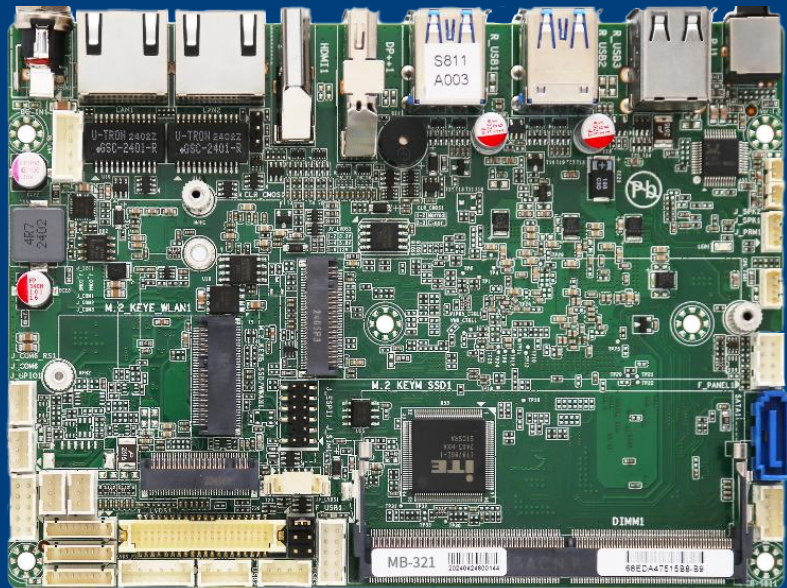




User Manual

Aicotek Motherboard | MB-321 User Manual

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1 Models and Attentions

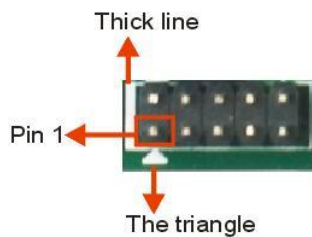
1.1 Model

This manual is applied to following models:

Model	CPU	COM	LAN	USB	DP++	HDMI	LVDS /eDP	M.2 Key-B	M.2 Key-E	M.2 Key-M	SATA 3.0
MB-321-N95	N95	6	2	9	1	1	LVDS	USB3.0+ USB2.0	PCIe+ USB2.0	PCIe/ SATA	1
MB-321-N97	N97	6	2	9	1	1	LVDS	USB3.0+ USB2.0	PCIe+ USB2.0	PCIe/ SATA	1
MB-321-N100	N100	6	2	9	1	1	LVDS	USB3.0+ USB2.0	PCIe+ USB2.0	PCIe/ SATA	1

1.2 Attentions

- 1) Notes under a table or figure indicate the difference of models, or alternative definition of specific pin of the header (jumper/connector).
- 2) How to identify the first pin of a header or jumper
 - Usually, there is a thick line or a triangle near the header's or jumper's pin 1.



- Square pad, which you can find on the back of the motherboard, is usually used for pin 1.



2 Specification

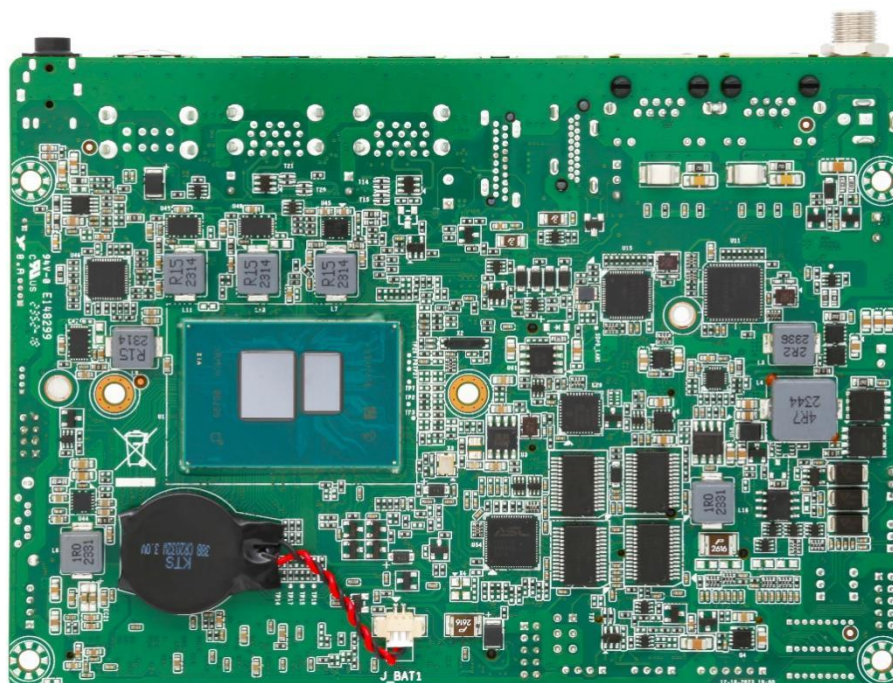
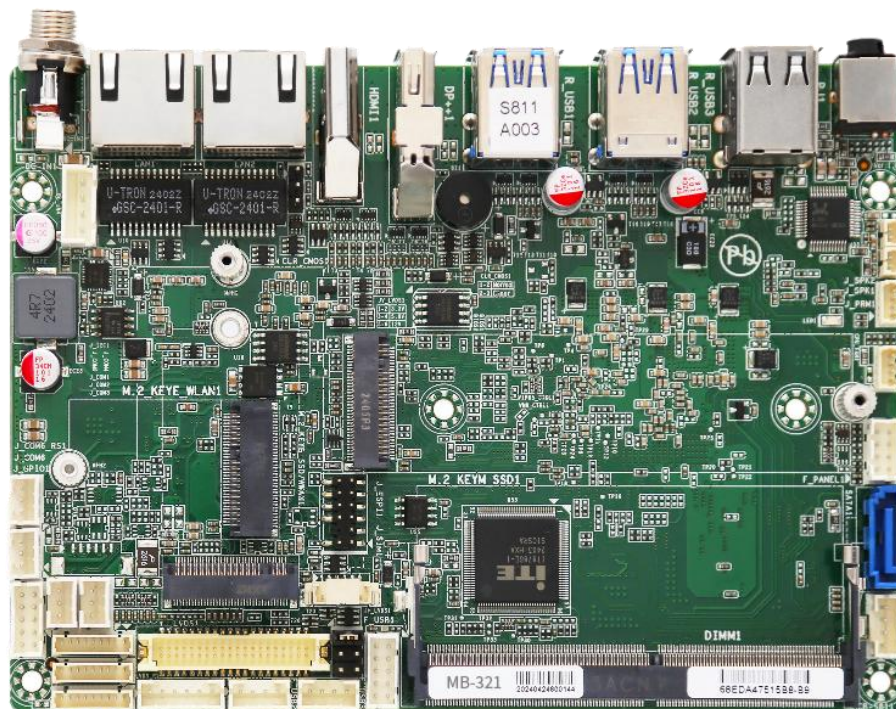
Specifications				
Model	Model	MB-321-N95	MB-321-N97	MB-321-N100
Processor System	Processor	Intel® Alder Lake-N Series Processor		
		N95	N97	N100
	Clock Speed	up to 3.40GHz	up to 3.60GHz	up to 3.40GHz
	Multi-Core	4E-Core	4E-Core	4E-Core
	TDP	15W	12W	6W
	BIOS	AMI UEFI BIOS (Support Watchdog Timer)		
Memory	Slot Type	1, DDR4 Non-ECC SO-DIMM		
	Memory Type	DDR4 3200MHz		
	Max Memory	16GB		
	Channels	Singal		
Display	Graphics	Intel® UHD Graphics		
		up to 16 EUs, 1.20 GHz	up to 24 EUs, 1.20 GHz	up to 24 EUs, 750 MHz
	HDMI	1, HDMI, max 4096*2160@30Hz		
	DP	1, DP++, max 4096*2160@60Hz		
		Notes: *: BOM optional support DP.		
	eDP/LVDS	1, LVDS, max 1920*1200@60Hz		
		Notes: *: BOM optional support eDP, max 4096*2160@60Hz		
	Multi-Display	Triple		
Audio	Codec	Realtek Audio HDA codec		
	Audio	1, Line-Out + MIC, CTIA		
		Notes: *: BOM optional support OMTP.		
	Amplifier	2, L/R Amplifier 3-W (per channel) into a 4- Ω Loads		
Storage	M.2 SSD	1, M.2 M-Key 2280, PCIE X1/SATA, Support PCIE X1 NVMe/SATA SSD, Auto Detect		

		Notice: *: BOM optional support PCIE X2/SATA. When support PCIE X2/SATA, M.2_KEYB_SSD/WWAN1 and SATA1 can't support SATA SSD.
	SATA SSD	1, SATA3.0 6Gbps Notice: *: SATA colay with M.2_KEYM_SSD1 and M.2_KEYB_SSD/WWAN1.
Expansion Slot	M.2	1, M.2 E-Key 2230, PCIE+USB2.0, support WiFi+ Bluetooth Module
		1, M.2 B-Key 2242/3052, USB3.0+ USB2.0, Support 5G/4G
		Notice: *: BOM optional support SATA, witch colay with M.2_KEYM_SSD1 and SATA1. *: USB2.0 signal colay with F_USB2.
	SIM Card	1, SIM Crad
Ethernet	Chipset	1, Intel i210-AT GbE Ethernet Controller 1, Intel i226-V GbE Ethernet Controller
USB	USB3.0	4, USB3.2 GEN1 5Gbps
	USB2.0	5, USB2.0
		Notice: *: BOM optional support F_USB2, witch colay with M.2_KEYB_SSD/WWAN1.
I/O	Serials	3, RS232 full Lines, COM1-3, DCD/5V and RI/12V selected by BOM, default DCD and RI 2, RS232/TTL 2 Lines, COM4-5, default RS232 1, RS232/TTL/RS485 2Lines, COM6, default RS232/RS485
	PANEL	1, PWR On +Reset +PWR_LED +HDD_LED
	Debug	1, ESPI
	FAN	1, CPU FAN
	I2C Touch	/
	CMOS Clear	1
GPIO	GPIO	4* GPI, 4* GPO, non-isolated 3.3V, 5V Optional
Power	Power in	DC 12V/19V/24V, Auto Detect 2 * DC 12V/19V/24V Power Input
		Notes: *: BOM optional support 24V or 12V.
OS	OS Supported	Windows 10/11 64bit, Linux
Environment	Temperature	Storage: -20 ~ 75°C

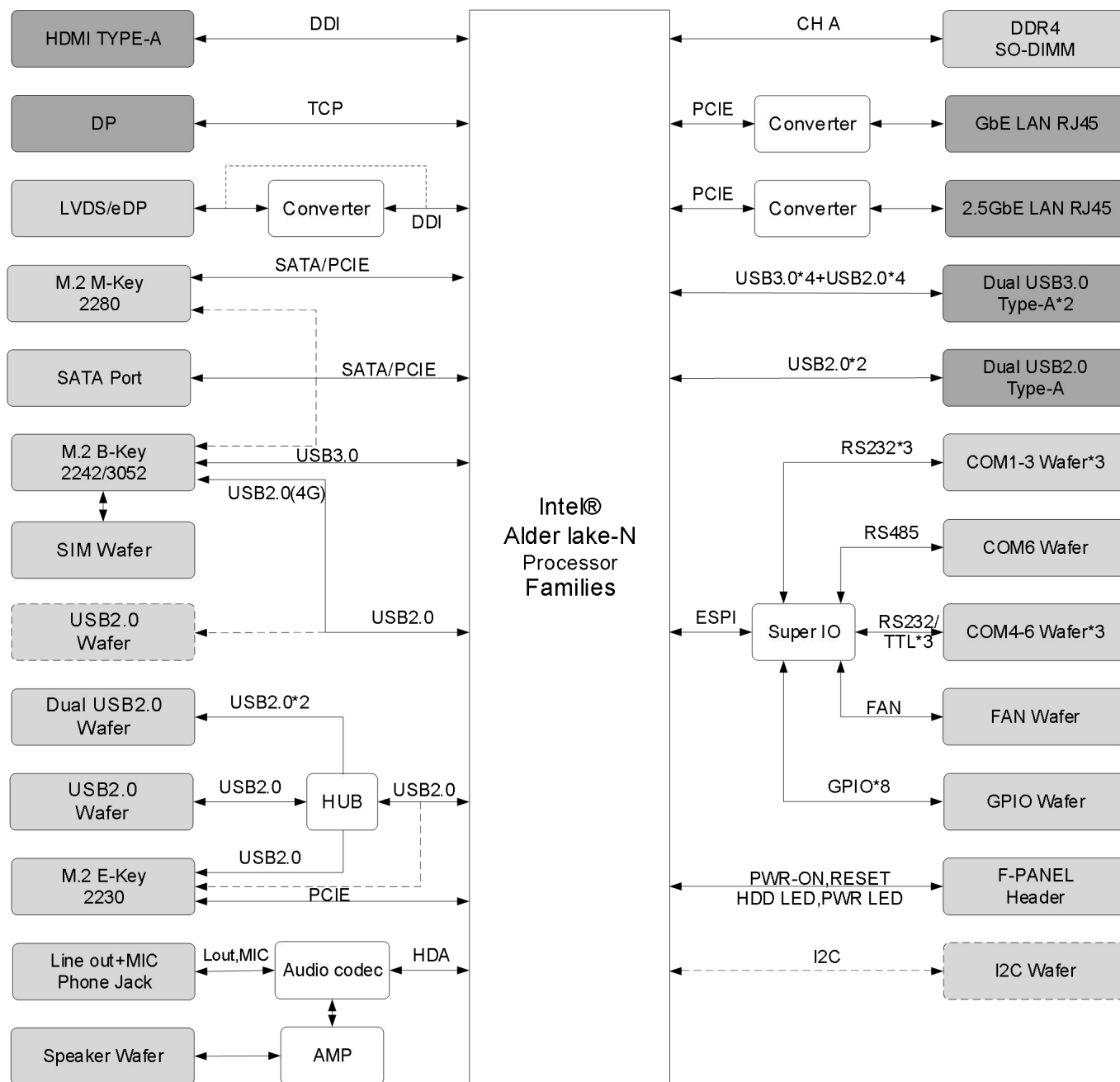
		Operation: -0 ~ 60°C
	Humidity	5 ~ 95%, non-condensing
Mechanical	Dimension	3.5 inch, 146mm*105mm
	Height	PCB: 1.6mm, Top side: H<19mm, Bot side: H<6.0mm

Interfaces

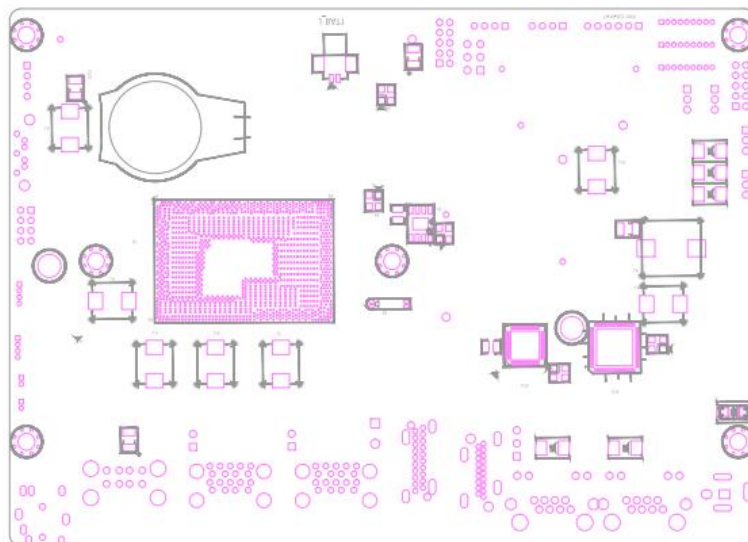
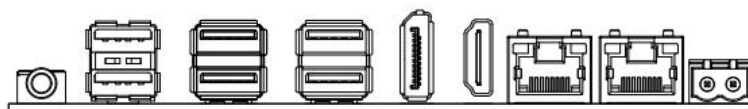
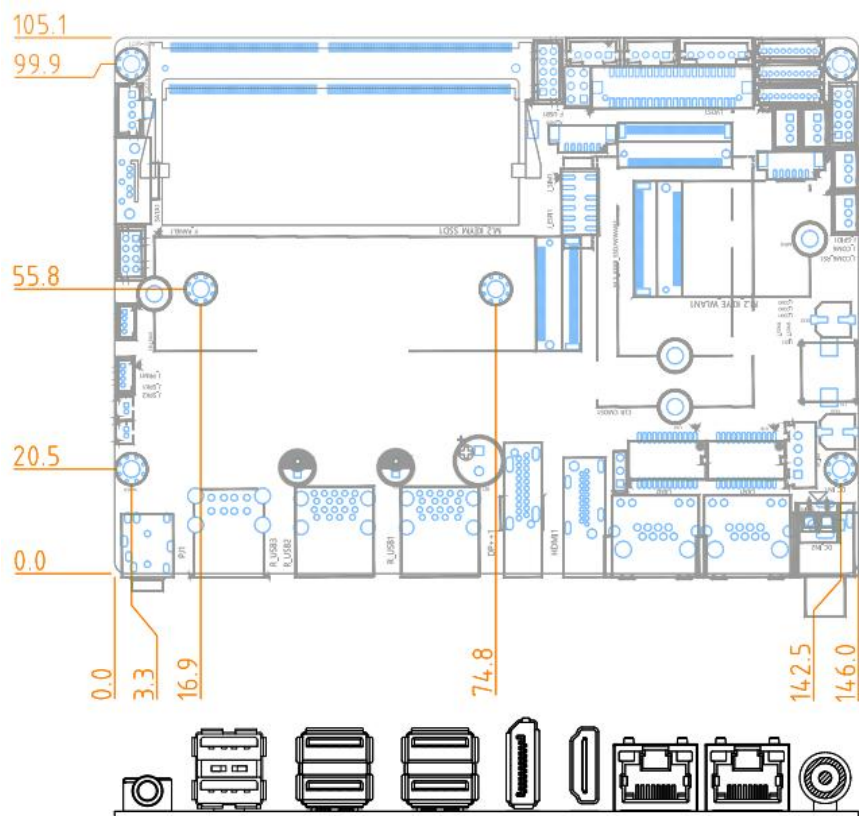
Model		MB-321-N95	MB-321-N97	MB-321-N100
Rear I/O	Audio	1, 2in1 Φ 3.5mm Jack		
	USB2.0	2, USB2.0 TYPE-A		
	USB3.0	4, USB3.0 TYPE-A		
	LAN	2, RJ45		
	DP	1, DP++ Port		
	HDMI	1, HDMI TYPE-A		
	Power In	1, Φ 2.5mm Thread Jack		
Internal I/O		Notes: *: BOM optional support 3.5mm/5.08mm 2P Terminal Block.		
	Display	1, DF13, eDP/LVDS, with Backlight Control Wafer		
	Power In	1, Wafer		
	Audio	2, Wafer, L/R Amplifier		
	Storage	1, SATA 7P Port, with power supply Wafer 1, M.2 M-Key 2280, PCIE/SATA		
	Expansion	1, M.2 E-Key 2230, PCIE+USB2.0, support WiFi+ Bluetooth Module 1, M.2 B-Key 2242/3052, USB3.0+ USB2.0, Support 5G/4G		
	USB2.0	3, Wafer		
	Serial	3, 9Pin Wafer, COM1-3, RS232 1, 3Pin Wafer, COM4-6, RS232/TTL 1, 3Pin Wafer, COM6, RS485		
	GPIO	1, Wafer		
	Front Panel	1, Wafer		
	FAN	1, Wafer		
	I2C Touch	/		
	Debug	1, Wafer, ESPI		
Others	Jumper	1, LVDS1 VDD Select 1, CMOS Clear Select		
	RTC	1, Wafer		
	Buzzer	1		



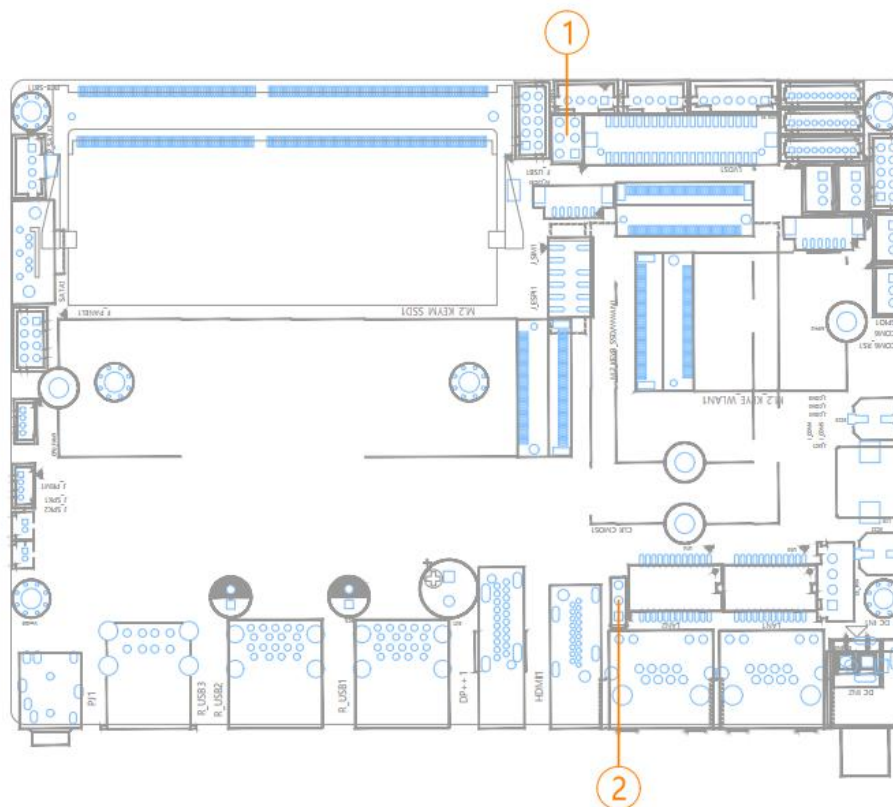
3 Block Diagram



4 Mechanical Drawing



5 Jumper



Jumpers / Headers and Connectors

①	JC_LVDS1	eDP/LVDS VDD Select Jumper
②	CLR_CMOS1	CMOS Clear Select Jumper

6 Definition of Jumpers

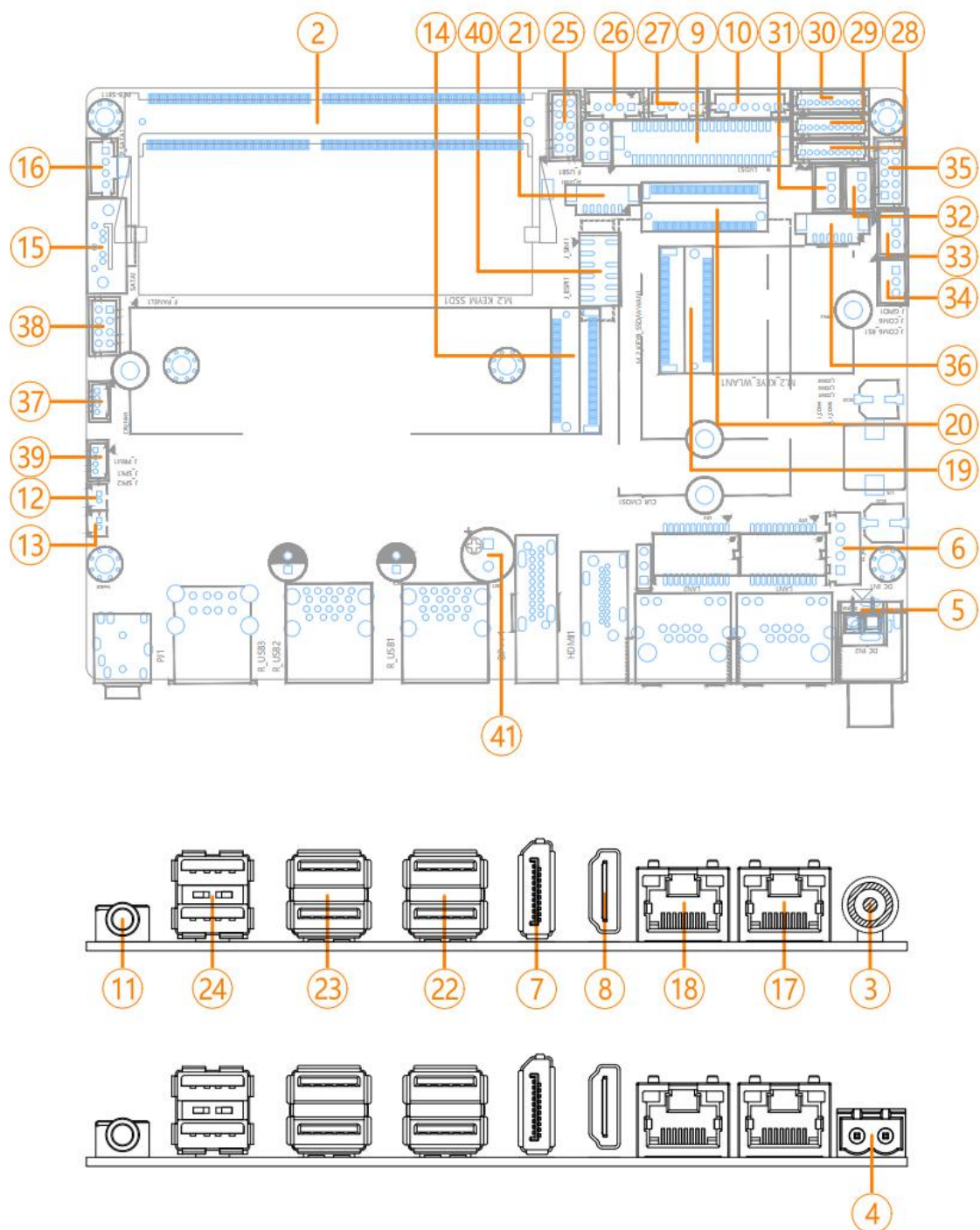
6.1 LVDS VDD Select: Jumper, 3*2P, 2.54mm (Mark No.1, JV_LVDS1)

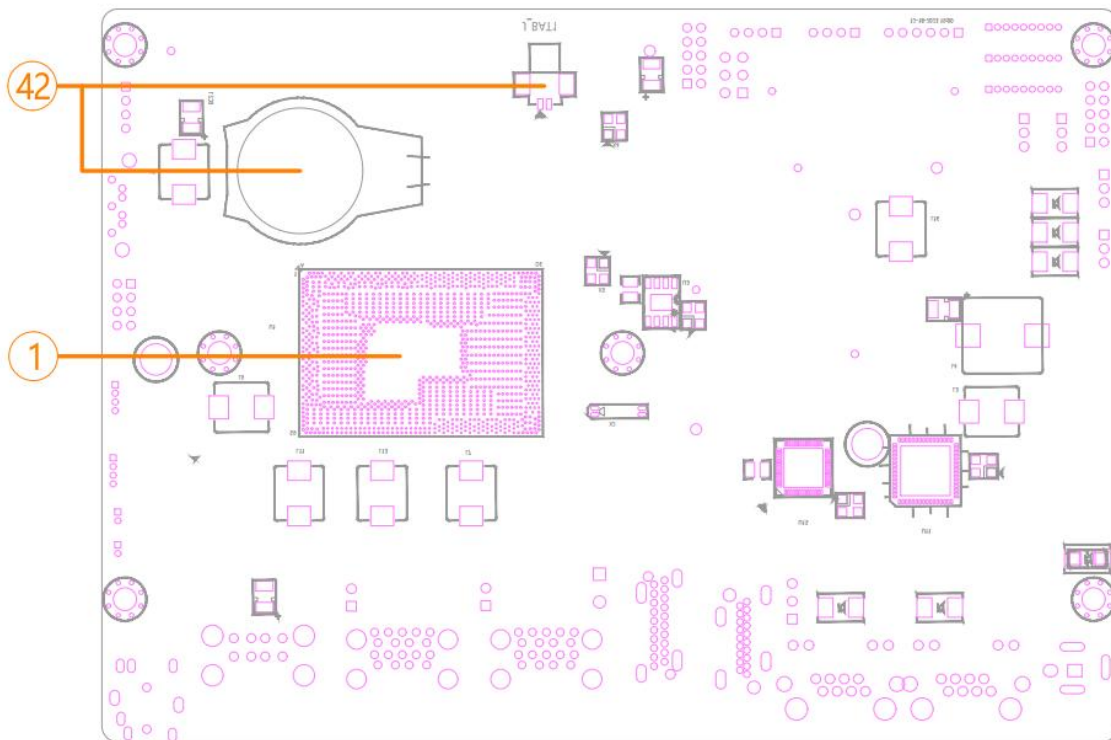
Graphic	Setting	Function
	1-2(Default)	VCC3.3
	3-4	VCC5
	5-6	VCC12

6.2 CMOS Clear: Jumper, 3*1P, 2.54mm (Mark No.2, CLR_CMOS1)

Graphic	Setting	Function
	1-2(Default)	Normal
	2-3	Clear CMOS

7 Headers / Wafers and Connectors





Jumpers / Headers and Connectors

①	U1	CPU
②	DIMM1	DDR4 CHA SO-DIMM Slot
③	DC_IN1	DC 12V/24V Power Input Φ 2.5mm Thread Jack
④	DC_IN3	DC 12V/24V Power Input 5.08mm 2P Terminal Block
⑤	DC_IN2	DC 12V/24V Power Input 3.5mm 2P Terminal Block
⑥	DC_IN4	DC 12V/24V Power Input Wafer
⑦	DP++1	DP++ Upright Connector
⑧	HDMI1	HDMI TYPE-A Connector
⑨	LVDS1	eDP/LVDS Signal Wafer
⑩	LVDS_P1	eDP/LVDS Backlight Control Wafer
⑪	PJ1	Line-Out + MIC 2in1 3.5mm Jack
⑫	J_SPK1	Right Amplifier Wafer
⑬	J_SPK2	Left Amplifier Wafer
⑭	M.2_KEYM_SSD1	M.2 M-Key Slot (PCIe x2/SATA, 2280)
⑮	SATA1	SATA3.0 7P Connector
⑯	P_SATA1	SATA Power Wafer
⑰	LAN1	GbE LAN RJ45 Connector
⑱	LAN2	GbE LAN RJ45 Connector

①9	M.2_KEYE_WLAN1	M.2 E-Key Slot (PCIE+USB2.0, 2230)
②0	M.2_KEYB_SSD/WWAN1	M.2 B-Key Slot (PCIE/SATA + USB3.0 + USB2.0, 2242/3052)
②1	J_SIM1	SIM Card Wafer
②2	R_USB1	Dual USB3.0 TYPE-A Connector
②3	R_USB2	Dual USB3.0 TYPE-A Connector
②4	R_USB3	Dual USB2.0 TYPE-A Connector
②5	F_USB1	Front Dual USB2.0 Wafer
②6	F_USB2	Front USB2.0 Wafer
②7	F_USB3	Front USB2.0 Wafer
②8	J_COM1	COM1 Wafer
②9	J_COM2	COM2 Wafer
③0	J_COM3	COM3 Wafer
③1	J_COM4	COM4 Wafer
③2	J_COM5	COM5 Wafer
③3	J_COM6	COM6 RS232/TTL Wafer
③4	J_COM6_RS1	COM6 RS485 Wafer
③5	J_GPIO1	Front GPIO Wafer
③6	J_I2C1	I2C Wafer
③7	CPU_FAN1	CPU FAN Wafer
③8	F_PANEL1	Front Panel Wafer
③9	J_PRM1	Power Debug Wafer
④0	J_ESPI1	ESPI Debug Header
④1	J_BAT1	CMOS Battery Wafer
④2	BZ1	Buzzer

8 Definition of Connectors

8.1 DC Power Input: Terminal Block, 2*1P, 5.08mm (Mark No.4, DC_IN3)

Graphic	Pin	Definition	Pin	Definition
 1	1	VCC_IN ^[1]	2	GND

Notes:

[1]: DC Power Input can be 24V, 12V or 12V/19V/24V, selectable by BOM.

8.2 DC Power Input: Terminal Block, 2*1P, 3.50mm (Mark No.5, DC_IN2)

Graphic	Pin	Definition	Pin	Definition
 1	1	VCC_IN ^[1]	2	GND

Notes:

[1]: DC Power Input can be 24V, 12V or 12V/19V/24V, selectable by BOM.

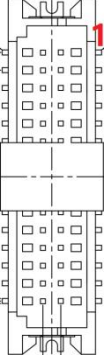
8.3 DC Power Input: Wafer, 4*1P, 2.54mm (Mark No.6, DC_IN4)

Graphic	Pin	Definition	Pin	Definition
 1	1	VCC_IN ^[1]	3	GND
	2	VCC_IN ^[1]	4	GND

Notes:

[1]: DC Power Input can be 24V, 12V or 12V/19V/24V, selectable by BOM.

8.4 eDP/LVDS Signal: Wafer, 20*2P, 1.25mm (Mark No.9, LVDS1)

Graphic	Pin	Definition	Pin	Definition
	1	VDD_PANEL ^[1]	2	VDD_PANEL ^[1]
	3	LVDS_PRSENT	4	GND
	5	VDD_PANEL ^[1]	6	VDD_PANEL ^[1]
	7	LVDS_A_DATA0-	8	LVDS_B_DATA0- /EDP1_TX0- ^[2]
	9	LVDS_A_DATA0+	10	LVDS_B_DATA0+ /EDP1_TX0+ ^[2]
	11	GND	12	GND
	13	LVDS_A_DATA1-	14	LVDS_B_DATA1- /EDP1_TX1- ^[2]
	15	LVDS_A_DATA1+	16	LVDS_B_DATA1+ /EDP1_TX1+ ^[2]
	17	GND	18	GND
	19	LVDS_A_DATA2-	20	LVDS_B_DATA2- /EDP1_TX2-

	21	LVDS_A_DATA2+	22	LVDS_B_DATA2+ / EDP1_TX2+
	23	GND	24	GND
	25	LVDS_A_CLK-	26	LVDS_B_CLK- /EDP1_TX3- ^[2]
	27	LVDS_A_CLK+	28	LVDS_B_CLK+ /EDP1_TX3+ ^[2]
	29	GND	30	GND
	31	N/C	32	EDP1_HPD_C
	33	GND	34	GND
	35	LVDS_A_DATA3-	36	LVDS_B_DATA3- / EDP1_AUX- ^[2]
	37	LVDS_A_DATA3+	38	LVDS_B_DATA3+ / EDP1_AUX+ ^[2]
	39	N/C	40	GND

Notes:

[1]: Panel Power VDD is 3.3V by default, 5V or 12V is selectable by “eDP/LVDS VDD Select Jumper”. (JV_LVDS1, Mark 8).

[2]: It supports LVDS by default and can support eDP if specified. (BOM selectable).

8.5 eDP/LVDS Backlight Control: Wafer, 6*1P, 2.00mm (Mark No.10, LVDS_P1)

Graphic	Pin	Definition	Pin	Definition
 1	1	GND	4	BKLT_EN
	2	GND	5	VCC12S
	3	BKLT_CTL	6	VCC12S

8.6 Right Amplifier: Wafer, 2*1P, 1.25mm (Mark No.12, J_SPK1)

Graphic	Pin	Definition	Pin	Definition
 1	1	SPK_R+	2	SPK_R-

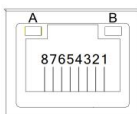
8.7 Left Amplifier: Wafer, 2*1P, 1.25mm (Mark No.13, J_SPK2)

Graphic	Pin	Definition	Pin	Definition
 1	1	SPK_L+	2	SPK_L-

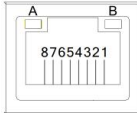
8.8 SATA Power: Wafer, 4*1P, 2.00mm (Mark No.16, P_SATA1)

Graphic	Pin	Definition	Pin	Definition
	1	VCC12	3	GND
	2	GND	4	VCC5

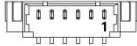
8.9 GbE LAN: RJ45 Connector (Mark No.17, LAN1)

Graphic	Pin	Definition		Pin	Definition	
	1	MDI0+		5	MDI2-	
	2	MDI0-		6	MDI1-	
	3	MDI1+		7	MDI3+	
	4	MDI2+		8	MDI3-	
	A	Active LED	ACT: Twinkling Yellow	B	Speed LED	1000M: Turn Yellow
			Only LINK: Lights On			100M: Turn Green
			Stop: Lights Off			10M: Lights Off

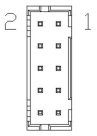
8.10 GbE LAN: RJ45 Connector (Mark No.18, LAN2)

Graphic	Pin	Definition		Pin	Definition	
	1	MDI0+		5	MDI2-	
	2	MDI0-		6	MDI1-	
	3	MDI1+		7	MDI3+	
	4	MDI2+		8	MDI3-	
	A	Active LED	ACT: Twinkling Yellow	B	Speed LED	1000M: Turn Yellow
			Only LINK: Lights On			100M: Turn Green
			Stop: Lights Off			10M: Lights Off

8.11 SIM Card: Wafer, 6*1P, 1.25mm (Mark No.21, J_SIM1)

Graphic	Pin	Definition	Pin	Definition
	1	UIM_PWR	4	UIM_CLK
	2	UIM_DATA	5	UIM_RST
	3	GND	6	UIM_VPP

8.12 Front USB2.0: Wafer, 5*2P, 2.00mm (Mark No.25, F_USB1)

Graphic	Pin	Definition	Pin	Definition
	1	VCC5	2	VCC5
	3	USB2.0_1-	4	USB2.0_2-
	5	USB2.0_1+	6	USB2.0_2+
	7	GND	8	GND
	9	GND	10	GND

8.13 Front USB2.0: Wafer, 4*1P, 2.00mm (Mark No.26, F_USB2)

Graphic	Pin	Definition	Pin	Definition
	1	VCC5	3	USB2.0+
	2	USB2.0-	4	GND

8.14 Front USB2.0: Wafer, 4*1P, 2.00mm (Mark No.27, F_USB3)

Graphic	Pin	Definition	Pin	Definition
	1	VCC5	3	USB2.0+
	2	USB2.0-	4	GND

8.15 COM1: Wafer, 9*1P, 1.25mm (Mark No.28, J_COM1)

Graphic	Pin	Definition	Pin	Definition
	1	PIN1 ^[1]	6	CTS
	2	DSR	7	DTR
	3	RXD	8	PIN9 ^[2]
	4	RTS	9	GND
	5	TXD		

Notes:

[1]: PIN1 can be DCD#/5V selectable by RES, support DCD# by default.

[2]: PIN9 can be RI#/12V selectable by RES, support RI# by default.

8.16 COM2: Wafer, 9*1P, 1.25mm (Mark No.29, J_COM2)

Graphic	Pin	Definition	Pin	Definition
	1	PIN1 ^[1]	6	CTS
	2	DSR	7	DTR
	3	RXD	8	PIN9 ^[2]
	4	RTS	9	GND
	5	TXD		

Notes:

[1]: PIN1 can be CTS#/5V selectable by RES, support DCD# by default.

[2]: PIN9 can be RI#/12V selectable by RES, support RI# by default.

8.17 COM3: Wafer, 9*1P, 1.25mm (Mark No.30, J_COM3)

Graphic	Pin	Definition	Pin	Definition
	1	PIN1 ^[1]	6	CTS
	2	DSR	7	DTR
	3	RXD	8	PIN9 ^[2]
	4	RTS	9	GND
	5	TXD		

Notes:

[1]: PIN1 can be CTS#/5V SEL by selectable, support DCD# by default.

[2]: PIN9 can be RI#/12V SEL by selectable, support RI# by default.

8.18 COM4: Wafer, 3*1P, 2.00mm (Mark No.31, J_COM4)

Graphic	Pin	Definition	Pin	Definition
	1	RXD	3	GND
	2	TXD		

8.19 COM5: Wafer, 3*1P, 2.00mm (Mark No.32, J_COM5)

Graphic	Pin	Definition	Pin	Definition
	1	RXD	3	GND
	2	TXD		

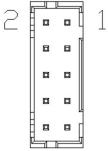
8.20 COM6: Wafer, 3*1P, 2.00mm (Mark No.33, J_COM6)

Graphic	Pin	Definition	Pin	Definition
	1	RXD	3	GND
	2	TXD		

8.21 COM6 RS485: Wafer, 3*1P, 2.00mm (Mark No.34, J_COM6_RS1)

Graphic	Pin	Definition	Pin	Definition
	1	RS485+	3	GND
	2	RS485-		

8.22 GPIO: Wafer, 5*2P, 2.00mm (Mark No.35, J_GPIO1)

Graphic	Pin	Definition	Pin	Definition
	1	SIO_GPI71 (0xA06 Bit1, H ^[1])	2	SIO_GPI70 (0xA06 Bit0, H ^[1])
	3	SIO_GPI73 (0xA06 Bit3, H ^[1])	4	SIO_GPI72 (0xA06 Bit2, H ^[1])
	5	SIO_GPO75 (0xA06 Bit5, H ^[1])	6	SIO_GPO74 (0xA06 Bit4, H ^[1])
	7	SIO_GPO77 (0xA06 Bit7, H ^[1])	8	SIO_GPO76 (0xA06 Bit6, H ^[1])
	9	GND	10	+3.3V ^[2]

Notes:

[1]: "H" or "L" means the default voltage is High or Low level (3.3V GPIO).

[2]: Power on this Pin is 3.3V by default, 5V is available if specified. (resistor selectable)

8.23 I2C: Wafer, 6*1P, 1.25mm (Mark No.36, J_I2C1)

Graphic	Pin	Definition	Pin	Definition
	1	VCC3.3	4	RST
	2	GND	5	SCL
	3	INT	6	SDA

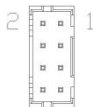
8.24 CPU FAN: Wafer, 4*1P, 1.25mm (Mark No.37, CPU_FAN1)

Graphic	Pin	Definition	Pin	Definition
	1	GND	3	FAN Speed Detection
	2	VCC12 ^[1]	4	FAN Speed Control

Notes:

[1]: Power on this Pin is 12V by default, 5V is available if specified. (resistor selectable)

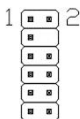
8.25 Front Panel: Wafer, 4*2P, 2.00mm (Mark No.38, F_PANEL1)

Graphic	Pin	Definition	Pin	Definition
	1	PWR LED+	2	HDD_LED+
	3	PWR LED-	4	HDD_LED-
	5	PWR On+	6	RESET-
	7	PWR On-	8	RESET+

8.26 Power Debug: Wafer, 4*1P, 1.25mm (Mark No.39, J_PRMI)

Graphic	Pin	Definition	Pin	Definition
	1	GND	3	VCCIN_SCL
	2	VCCIN_PE	4	VCCIN_SDA

8.27 ESPI Debug: Header, 6*2P, 2.00mm (Mark No.40, J_ESPI1)

Graphic	Pin	Definition	Pin	Definition
	1	ESPI_I00	2	VCC3.3
	3	ESPI_I01		
	5	ESPI_I02	6	ESPI_CLK
	7	ESPI_I03	8	GND
	9	ESPI_CS0-	10	VCC3.3
	11	ESPI_ALERT0_N	12	PLTRST_N ^[1]

Notes:

[1]: Signal on this Pin is PLT_RST_N by default, ESPI_RST0_N is available if specified. (resistor selectable).

8.28 CMOS Battery: Wafer, 2*1P, 1.25mm (Mark No.41, J_BAT1)

Graphic	Pin	Definition	Pin	Definition
	1	VCC_BAT	2	GND

【End】



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